FEATURES

- A UNIQUE (Patent Pending) TECHNIQUE FOR VERY LOW QUIESCENT CURRENT
- OVER 350 V/µS SLEW RATE
- WIDE SUPPLY VOLTAGE
  - Single Supply: 20V to 350V
  - Split Supplies: +/– 10V to +/– 175V
- OUTPUT CURRENT – Per Amplifier – 150mA cont. ; 200mA Pk
- UP TO 26 WATT DISSIPATION CAPABILITY (DUAL)
- OVER 200 kHz POWER BANDWIDTH

APPLICATIONS

- PIEZOELECTRIC POSITIONING AND ACTUATION
- ELECTROSTATIC DEFLECTION
- DEFORMABLE MIRROR ACTUATORS
- CHEMICAL AND BIOLOGICAL STIMULATORS

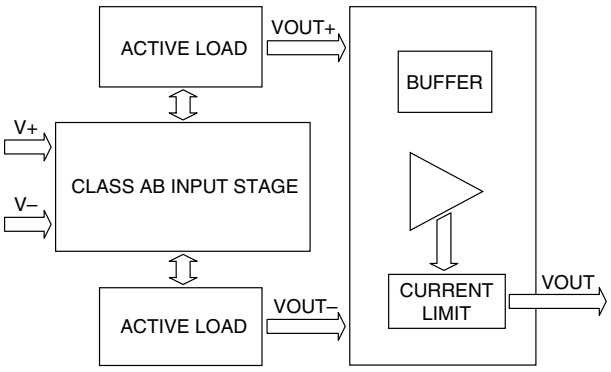
DESCRIPTION

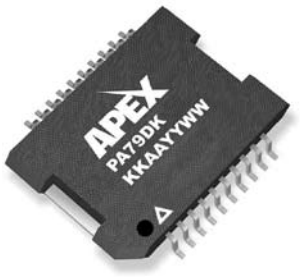
The PA79 is a dual high voltage, high speed Precision IC power op amp with performance and unique features not found previously in any commercially available OpAmp. This approach provides a cost-effective, high density solution to applications where multiple amplifiers are required.

Novel input stage design of this amplifier provides extremely high slew rates in pulse applications while maintaining low quiescent current of under 1mA. This novel input stage also has the effect of adding variables to the power response and slew rate characteristics of the amplifier. To a lesser degree, there are also input related effects on unity gain bandwidth and phase. It is important to note that the slew rate is a strong function of input voltage amplitude. **It should be noted that the package tab needs to be connected to a stable reference such as GND for high slew rates. Please refer to special considerations section for details.**

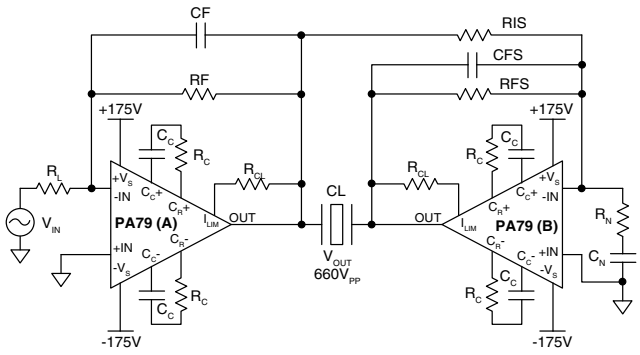
The output stages are well protected with user defined current limit although the Safe Operating Area (SOA) must be observed for reliable protection. Proper heatsinking is required for maintaining maximum reliability. External phase compensation provides the user with great flexibility in trading gain, stability and bandwidth.

BLOCK DIAGRAM





20–PIN PSOP
PACKAGE STYLE DK



TYPICAL APPLICATION

The typical application diagram shows a bridge connection of the two amplifiers inside a dual PA79 and provides output voltage swing twice that of one amplifier. Two possible situations where there is an advantage would be in applications with low supply voltages, or applications that operate amplifiers near their maximum voltage ratings in which a single amplifier could not provide sufficient drive. The bridge connection also effectively doubles the slew rate, and non-linearity becomes

ABSOLUTE MAXIMUM RATINGS

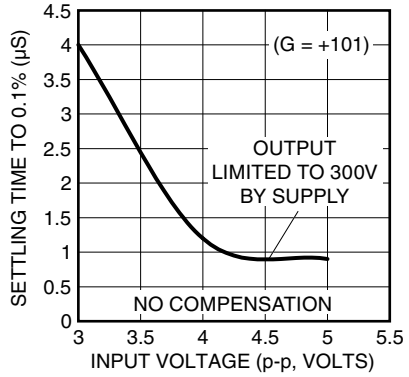
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, peak (200ms)	200mA, within SOA
POWER DISSIPATION, internal, DC	14W Single
POWER DISSIPATION, internal, DC	26W Dual
INPUT VOLTAGE, Differential	±15V
INPUT VOLTAGE, Common Mode	±Vs
TEMPERATURE, junction[2]	150°C.
TEMPERATURE RANGE, storage	–55 to 125°C
OPERATING TEMPERATURE, case	–40 to 125°C

SPECIFICATIONS

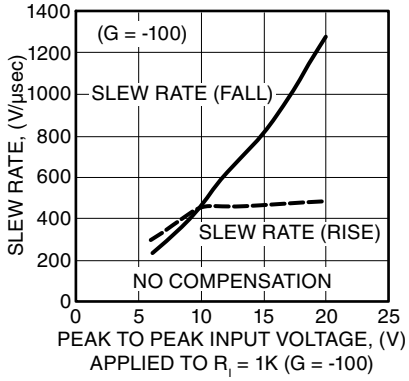
PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE		–40	8	40	mV
OFFSET VOLTAGE vs. temperature	0 to 125°C (CaseTemperature)		–63		µV/°C
OFFSET VOLTAGE vs. supply				32	µV/V
BIAS CURRENT, initial			8.5	200	pA
OFFSET CURRENT, initial			12	400	pA
INPUT RESISTANCE, DC			10^8		Ω
COMMON MODE VOLTAGE RANGE, pos.			$+V_S - 2$		V
COMMON MODE VOLTAGE RANGE, neg.			$-V_S + 5.5$		V
COMMON MODE REJECTION, DC		90	118		dB
NOISE	700KHz		418		µV RMS
NOISE, V_ONOISE			500		nV/√Hz
GAIN					
OPEN LOOP @ 1Hz		89	120		dB
GAIN BANDWIDTH PRODUCT @ 1MHz			1		MHz
PHASE MARGIN	Full temperature range		50		°
OUTPUT					
VOLTAGE SWING	I_O = 10mA		$\|V_S\| - 2$		V
VOLTAGE SWING	I_O = 100mA		$\|V_S\| - 8.6$	$\|V_S\| - 12$	V
VOLTAGE SWING	I_O = 150mA		$\|V_S\| - 10$		V
CURRENT, continuous, DC		150			mA
SLEW RATE	**Package Tab Connected to GND**	100	350		V/µS
SETTLING TIME, to 0.1%	5V Step (No Compensation)		1		µS
POWER BANDWIDTH, $300V_{P-P}$	$+V_S$ = 160V, $-V_S$ = –160V		200		kHz
OUTPUT RESISTANCE, No Load	R_{CL} = 6.2Ω		44		Ω
POWER SUPPLY					
VOLTAGE		±10	±150	±175	V
CURRENT, quiescent[5]	±150V Supply	0.2	0.7	2.5	mA
THERMAL					
RESISTANCE, DC, junction to case, dual[8]	Full temperature range		4.4	4.8	°C/W
RESISTANCE, DC, junction to case, single	Full temperature range		8.3	9.1	°C/W
RESISTANCE, junction to air	Full temperature range		25		°C/W
RESISTANCE, junction to air	Full temperature range		19.1		°C/W
TEMPERATURE RANGE, case		–40		125	°C

NOTES:
1. Unless otherwise noted: TC = 25°C, DC input specifications are ± value given, power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative supply voltages of the output stage.
4. Rating applies if output current alternates between both output transistors at a rate faster than 60Hz.
5. Supply current increases with signal frequency. See graph on page 4. Applies to each amplifier.
6. Rating applies when the heatslug of the DK package is soldered to a minimum of 1 square inch foil area of a printed circuit board.
7. Rating applies with the JEDEC conditions outlined in the Heatsinksing section of this datasheet.
8. Rating applies when power dissipation is equal in two amplifiers.

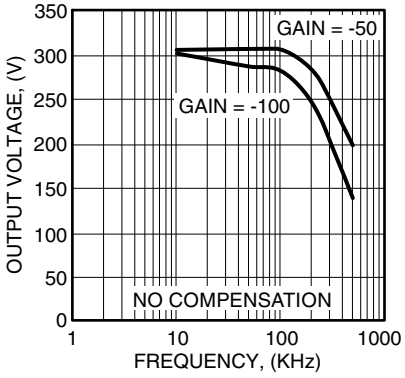
SETTLING TIME TO 0.1 % OF 300V



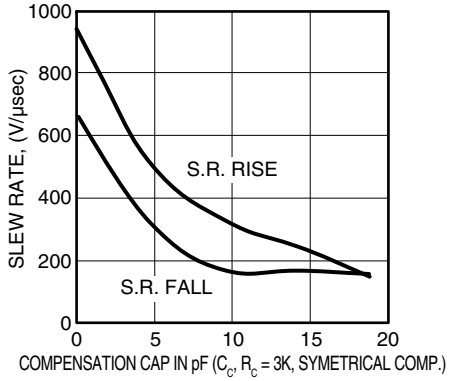
SLEW RATE vs. INPUT VOLTAGE



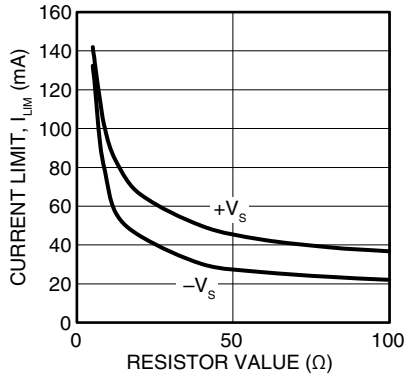
POWER RESPONSE



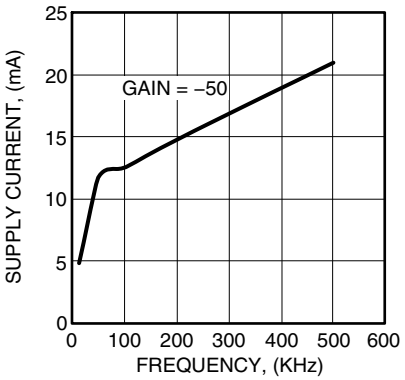
SLEW RATE vs. COMPENSATION CAP.



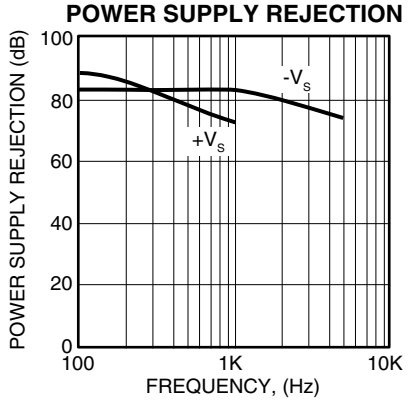
CURRENT LIMIT



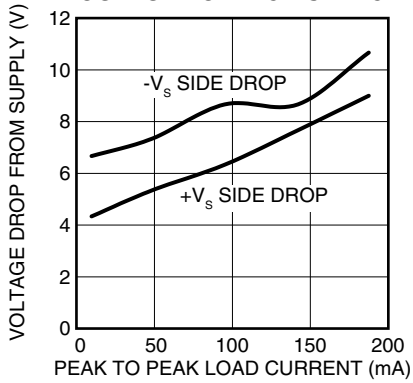
SUPPLY CURRENT vs. FREQUENCY



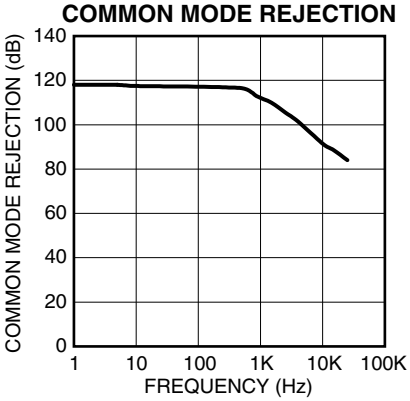
POWER SUPPLY REJECTION



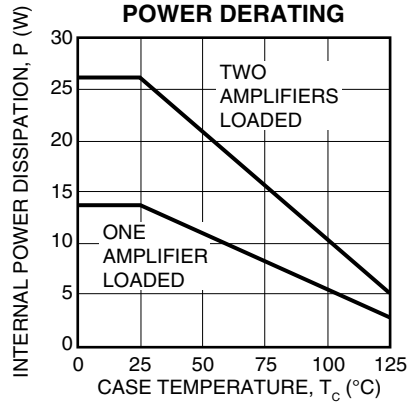
OUTPUT VOLTAGE SWING



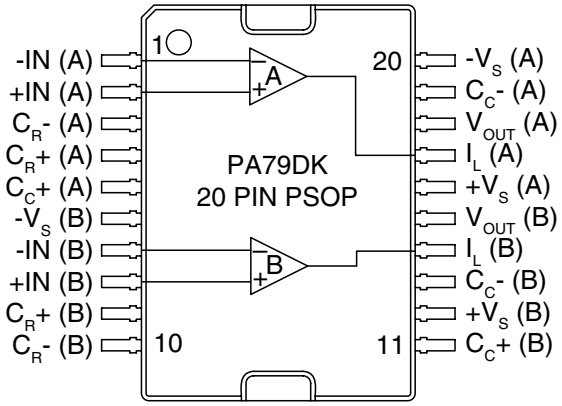
COMMON MODE REJECTION



POWER DERATING



EXTERNAL CONNECTIONS



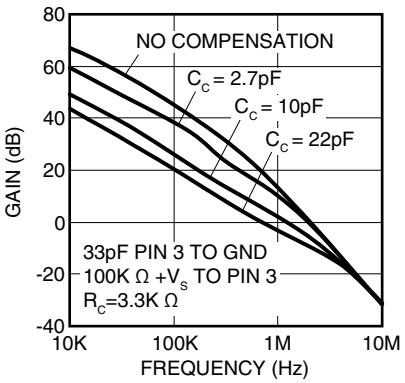
NOTES:

1. The package heat slug needs to be connected to a stable reference such as gnd for high slew rates. Please refer to special considerations section for details.
2. Supply bypassing required for –Vs and +Vs.
3. For Cc and Rc values refer to power supply biasing section.
4. Dimple and ESD triangle denotes pin 1.

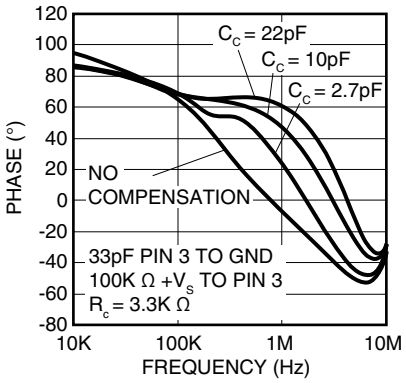
SMALL SIGNAL GAIN AND PHASE PLOTS

The input signal amplitude to the PA79 amplifier is related to the overall phase margin and unity gain bandwidth. For very small signal amplitudes the amplifier phase margin is negative and it shows instability. If small signal stability is desired a constant current source of 500 uA (or resistor for constant supply voltage) needs to be added externally between C_C– and +V_S. This current source has minor effects on output offset voltage but helps immensely with small signal stability. The following gain and phase plots have been generated with a 100k resistor (fixed dual supply voltage +/– 50V) between C_C– and +V_S. Please note that the unity gain bandwidth and phase margin improves with larger signal amplitude because of the unique differential amplifier stage in the PA79.

OPEN LOOP GAIN



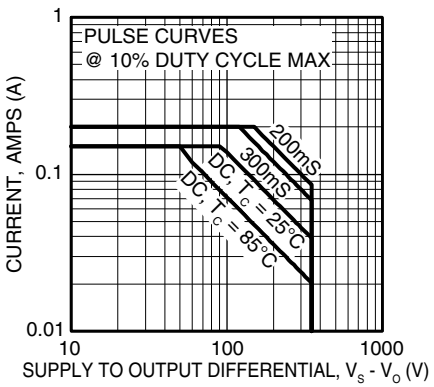
PHASE RESPONSE



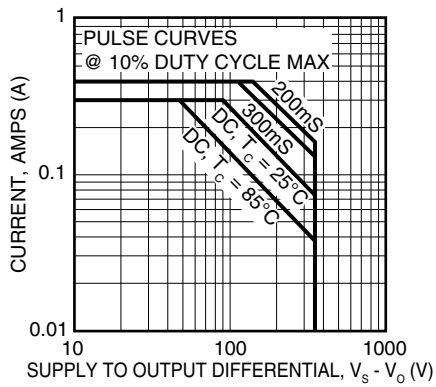
SAFE OPERATING AREA

The MOSFET output stage of the PA79 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA. The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast–recovery diodes must be used.

SINGLE AMPLIFIER SOA



DUAL AMPLIFIER SOA



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

SPECIAL CONSIDERATIONS

It is very important to realize that in order to achieve high frequency performance the heat sink tab has to be tied to a stable, low impedance reference, i.e. power supply or GND. An AC connection through a 0.1µF capacitor is also sufficient. Internal to the PA79, the heatsink tab is electrically isolated to more than 350V . This may help allay some electrical isolation concerns in tying the heat sink to Vs or GND.

CURRENT LIMIT

For proper operation, the current limit resistor, R_{LIM}, must be connected as shown in the external connections diagram. For maximum reliability and protection, the resistor should be set as high as possible. The maximum practical value using the following formula is 12 ohms. For even lower current limit values, please see the CURRENT LIMIT vs. RESISTOR graph on the TYPICAL PERFORMANCE GRAPHS page.

$$R_{LIM} = 0.7 / I_{LIM}$$

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals +Vs and –Vs must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the PA79. Use high quality ceramic capacitors (X7R) 0.1µF or greater.

SUPPLY CURRENT

The PA79 features a class A/B driver stage to drive the output MOSFETs and an innovative input stage to achieve very high slew rates. The supply current drawn by the PA79, even with no load, varies with the slew rate of the output signal.

MOISTURE SENSITIVITY

The PA79DK has been qualified according to JEDEC 22-A-113-D, MSL 3. The following conditions were used: IR reflow for Pb-free assembly profile where: package thickness is greater than 2.5mm, package volume is greater than 350mm^2, TP = 245°C.

HEATSINKING

The PA79DK package has a large exposed integrated copper heatslug to which the monolithic amplifier is directly attached. The solder connection of the heat slug to a 1 square inch foil area on the printed circuit board will result in improved thermal performance of 25C/W. In order to improve the thermal performance, multiple metal layers in the printed circuit board are recommended. This may be adequate heatsinking but the large number of variables involved suggest temperature measurements be made on the top of the package. Do not allow the temperature to exceed 85°C.

The junction to ambient thermal resistance of the DK package can achieve a 19.1C/W rating by using the PCB conditions outlined in JEDEC standard: (JESD51–5):

PCB Conditions:
- PCB Layers = 4L, Copper, FR–4
- PCB Dimensions = 101.6 x 114.3mm
- PCB Thickness = 1.6mm

Conditions:
- Power dissipation = 2 watt
- Ambient Temperature = 55°C

STABILITY

The PA79 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. Due to the innovative design of the PA79, two compensation networks are required. The values of these components should be the same to provide symmetric slew rate characteristics. The compensation capacitor Cc must be rated at 500V working voltage. NPO capacitors are recommended. The compensation networks CcRc must be mounted closely to the amplifier pins 8 & 11 and 3 & 10 to avoid spurious oscillation.

The PA79 may require an external 33 pF capacitor (minimum breakdown of 350V) between Cc– and –Vs to prevent oscillations in the falling edge of the output. This capacitor is provided with the evaluation kit. Please refer to EK60U datasheet for details.

ELECTROSTATIC DISCHARGE

Like many high performance MOSFET amplifiers, the PA79 very sensitive to damage due to electrostatic discharge (ESD). Failure to follow proper ESD handling procedures could have results ranging from reduced operating performance to catastrophic damage. Minimum proper handling includes the use of grounded wrist or shoe straps, grounded work surfaces. Ionizers directed at the work in progress can neutralize the charge build up in the work environment and are strongly recommended.

